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Synchronization control techniques for shunt active power filter: an overview

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Article Info	ABSTRACT
	The phase synchronization control technique of shunt active power filter (SAPF) is discussed in this article. Due to the harmful effects of harmonic currents on power systems, the issue of decreasing their effects has generated a lot of research. A SAPF is acknowledged as the most dependable instrument in this area. The SAPF will detects the current harmonics present in the power system and also generates and injects the corrective current mitigation in the power system to reduce the current harmonics. This implies that, aside from the capacity to create compensating current, it is more essential to ensure that the SAPF can work in phase with the operational power system so that the compensating current will properly injected. As a result, while constructing SAPF control algorithms, correct synchronisation techniques must be incorporated. In this article, the different types of phase synchronization approach have been discussed such as phase-locked loop (PLL), adaptive linear neuron (Adaline), and unit vector. The results of the study may be used as a guideline and source of information for determining the best method for synchronising SAPF with the associated power system.

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1. INTRODUCTION

The nonlinear loads' widespread use has resulted in serious issues of power quality, primarily harmonic degradation problems in the electrical distribution systems. In general, the current harmonics can reduce the power quality of the system by raising the total harmonic distortion (THD). Moreover, the current harmonics are the main source for decreasing the efficiency of the system overheating of the system, and failure of system devices [1]–[3]. To protect the system from the failure and maintain harmonic in the electrical system within a prescribed limit, a passive filter play the important role in electrical distribution system.

To solve a specific harmonic problem, harmonic filters are usually constructed with passive filters such as inductors and capacitors [4]–[6]. But, passive filters are good enough to filter out a certain harmonic order. In other hand, these kinds of filters are suffered with tuning and harmonic resonance problems and large filter size requirement as well. To solve the problems of the conventional passive filter, a shunt active power filter (SAPF) approach is adapted by the various authors in the literature [7]. However, active power filters (APFs), which provide a variety of solutions to harmonic problems, quickly replace these due to their intrinsic faults [8]. APF technology is advancing because of its greater mitigating capabilities. APFs are currently accessible in a variety of forms that may be divided into many broad groups. According to Anzalchi *et al.* [9], APF can be classified based on i) connection to the power system, ii) power rating, iii)

types of power converter employed, iv) power converter employed, and v) characteristics of power system. Nonetheless, as evidenced by the literature [10]. SAPF are the generally valuable filter for the reduction of harmonic currents.

The SAPF is measuring the current harmonic contamination of the power system, and provides the corrective current mitigation to the harmonic power system to decrease the harmonics in the system. However, the use of SAPF in distribution network has the difficulties of synchronization. The phase synchronization is one of the most significant concerns, In order to provide steady and continuous mitigation ability, the generated output voltage must be precisely coordinated with the grid voltage [11].

In this context, phase synchronization can be defined as the process of reducing phase differences between the grid voltage and the SAPF output voltage while also matching the operational frequencies [12], [13]. Before connecting the SAPF to the chosen power system, this step must be done in order for the power system and the synchronised SAPF to work together and control techniques are discussed in details [14]. In order to overcome the challenges and problems associated with phase synchronisation, different methods with specific advantages for synchronising grid-connected inverters have been presented. In this article, the numerous types of phase synchronization methods are applied to the SAPF is discussed in details [15]. Researchers should be able to use the findings of this study to help them choose the best synchronization method for their SAPF, and it may even inspire them to come up with new ideas for enhancing SAPF synchronizing.

The block diagram of voltage source inverter based SAPF with non-linear load is given in Figure 1. The SAPF consists of four control algorithms to control the system. Normally, the SAPF is connected between the source and non-linear load at pearson correlation coefficient (PCC) to reduce the harmonics. From literature, the harmonic producing loads are commonly used uncontrolled bridge rectifier with the combination of resistor, inductor, and capacitor [16], [17]. The block diagram of SAPF has two parts: i) power converter with power semi-conductor switches and ii) control circuit to operate the switches.
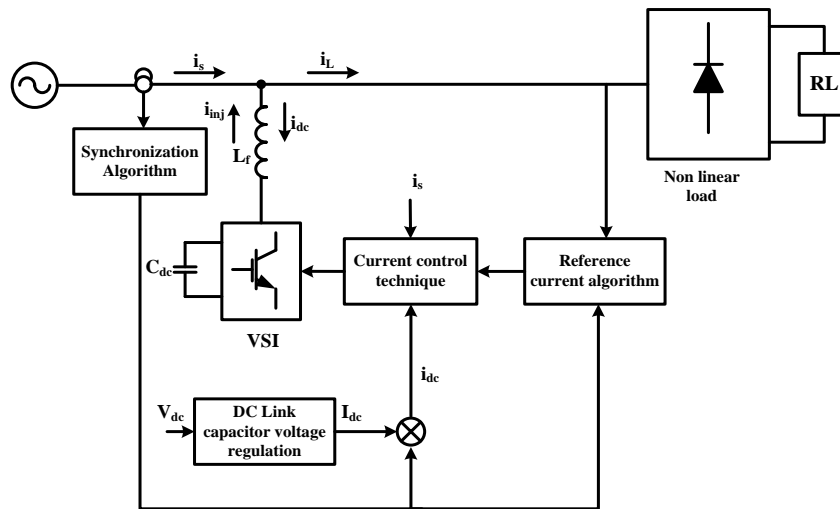

Figure 1. Block diagram of SAPF

The SAPF working is very simple and easy to control. The advantages of SAPF are reduction of harmonics, power factor improvement, DC voltage regulation, elimination of resonance in the system [18]. At PCC, by applying Kirchhoff's current law (KCL), the harmonic current is polluting the system during the absence of SAPF. The source current is affecting due to harmonics [19] and it is given as in (1).

$$i_S = i_L = i_{fL} + i_H \qquad (1)$$

Where i_S is source current, i_L is load current, i_{fL} is fundamental current, i_H is harmonic current. Note that the all current are generated by the non-linear loads. At this junction load current and source voltage is may not be in-phase.

Now, the SAPF is installed at PCC, and then the two currents are flown in the system [20]. First, the injecting harmonic current i_{inj} is injected by SAPF to reduce the current harmonic si_H. Second, DC-link current i_{dc} which is used to continue constant dc voltage v_{dc}. Therefore, the source current i_S is given as in (2).

$$i_S = (i_{fL} + i_H) - i_{inj} + i_{dc} \tag{2}$$

By theoretical, the injected harmonic current i_{inj} is affected by dc-link voltage of capacitor. When voltage reaches to the preferred level, then injected current will be same as harmonic current i_H, they cancel out by themselves and (2) can be written as.

$$i_S = i_{fL} + i_{dc} \tag{3}$$

At this point, by removing harmonic current i_H, the source current i_S is regained its natural sinusoidal structure and i_S is in-phase with v_S. Four different types of control algorithms must be introduced into the control system of the SAPF in order to successfully manage its operations.

a. Harmonic extraction algorithm: this algorithm's primary purpose is to excerpt harmonic data from a power system that has been harmonically polluted. The collected data is then used to create a reference current signal, abbreviated iref. A few examples of frequently used strategies for this algorithm are the synchronous reference frame (SRF) or discrete quantum theory (dq theory) [21], instantaneous power pq theory [22], fast fourier transform (FFT) [23], and artificial neural network (ANN) [24], [25].

b. Synchronization algorithm: this algorithm's primary job is to track the angle of the source voltage signal VS and then produce a phase synchronisation angle to align the phase of the generated ire f with the phase of the running power system. As an illustration, consider the algorithm developed using the instantaneous power pq theory technique [26].

c. DC-link capacitor voltage regulation algorithm: this algorithm's primary purpose is to determine how much dc-link charging current idc the SAPF will require to continuously maintain a specific level of dc-link voltage volt direct current (Vdc).

d. Current control algorithm: this algorithm's primary job is to pulse-width modulate ire f from the harmonic extraction algorithm and idc from the dc-link capacitor voltage regulation algorithm into gate switching pulses S such that the feedback signal i_{inj} or i_S can follow ire f via a current control loop. Hysteresis control [27], sinusoidal pulse-width modulation (SPWM) [28], and space vector PWM (SVPWM) [29] are a few examples of regularly used algorithms for this methodology.

The actual output (which might be either i_{inj} or i_S) is observed and supplied back to be compared with the desired one until the monitored output achieves its required response. The four control algorithms are connected to one another in a systematic way. The algorithms have been demonstrated in practise to be capable of responding swiftly to disturbances like dynamic situations in order to restore the monitored output to the desired shape once more.

2. SYNCHRONIZATION TECHNIQUES

At operational frequencies, synchronization is the process of minimizing phase deviations between the SAPF voltage and grid voltage. This voltage should be tracked, frequency fluctuations should be detected, higher order harmonics should be filtered out, and grid voltage variations should be responded to the variations. The different types of synchronization techniques are shown in Figure 2.
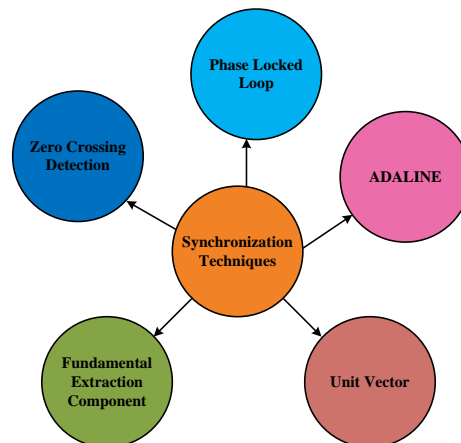

Figure 2. Synchronization techniques classifications

2.1. Zero correlation duration approach

For the phase synchronization, zero correlation duration (ZCD) is playing a very important role for the solving of phase detection [30], [31]. The function of ZCD technique is generating the switching pulses by detecting the zero-crossing point of AC voltage signal. It provides the highest benefits in terms of implementation requirements, but it fails to work in practise, particularly while the source voltage is disturbed or subjected to harmonics. In such cases, multiple zero crossings may occur, making it more difficult for the zero-crossing detector to detect the original zero crossing and perhaps causing to false detection. A ZCD hardware circuit is designed to give an initiating pulse to the SAPF controller when a zero-crossing voltage is detected at the PCC, for example, in [32]. The initial pulse acts as a toggle, allowing the controller to initiate the operation. This approach can be used with single-phase or three-phase systems [33]. Nonetheless, due to its shortcomings, this approach is still the least recommended for SAPF application implementation when compared to the other accessible ways.

2.2. Phase locked loop technique

The phase locked loop (PLL) approach is extensively used solution because of its simple control structure and efficiency in coping with a variety of grid conditions. PLL techniques is effective implemented in a wide range of applications namely, control systems, communications, and instrumentation. Figure 3 gives the control structure of PLL, and it comprise the various blocks such as voltage-controlled oscillator (VCO), loop filter and phase detector. Initially, the phase detector [34] detects the phase error signal $\Delta\theta$ by comparing the reference phase signal θ_{ref} with the feedback signal θ. The generated error signal $\Delta\theta$ is passed through the loop filter to supress the high frequency noise signals. The filtered signal is now processed towards the VCO to obtain the modified phase angle θ which is acting as feedback to the phase detector. As continuous loop process, the value of error is reduced and reaches to the zero value, which produces the desired reference signal θ_{ref}.
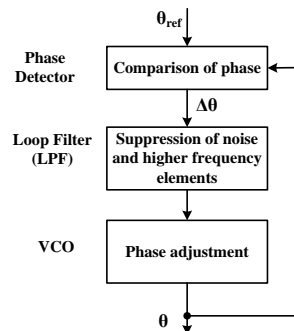

Figure 3. Control structure of PLL

The SRF-PLL [35] structure is most preferred synchronisation technique for the applications of three phase SAPF. The control structure of SRF-PLL technique is given in Figure 4. Initially, the three-phase voltage V_{Sabc} is converted into two phase $\alpha\beta$ stationary frame using clarke's transformation as given in (4).

$$\begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{Sa}(k) \\ v_{Sb}(k) \\ v_{Sc}(k) \end{bmatrix} \tag{4}$$
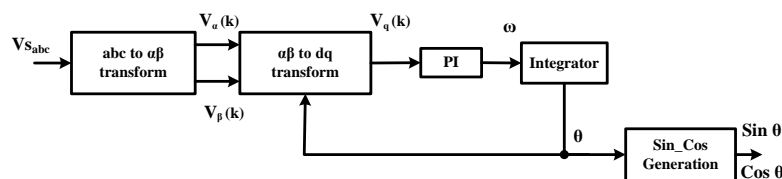

Figure 4. Structure of SRF-PLL

The αβ stationary frame [36] is now converted into dq rotating reference frame using park's transformation as given in (5).

$$\begin{bmatrix} v_d(k) \\ v_q(k) \end{bmatrix} = \begin{bmatrix} Cos\theta & Sin\theta \\ -Sin\theta & Cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix}$$

(5)

The resultant q variable is then controlled by a proportional-integral (PI), and the utility's angular frequency is produced as the output. By integrating the angular frequency and then feeding it back into the dq transformation until the phase angle is set at a constant value, the utility phase angle can be obtained. In case of abnormal conditions such as unbalanced voltages and distortions in voltage sources due to harmonics, the SRF-PLL technique fails to track the utility's angular frequency quickly and allows for precise phase angle measurement. When the source voltage is devoid of distortions and imbalances, the fundamental benefit of the SRF-PLL technique is that it enables exact and quick monitoring of utility frequency and phase angle. Sadly, the SRF-PLL malfunctions when the supplied voltage is unbalanced and/or distorted as a result of harmonics.

2.3. Adaptive linear neuron synchronization approach

The concept of the adaptive linear neuron (Adaline) [37] is one current synchronisation method (Adaline). To extract harmonics or generate reference current, the Adaline method is first introduced [38], [39]. Furthermore, the Adaline technique for harmonic extraction has been suggested for SAPF synchronisation with adequate consideration. In this context, unified Adaline strategy is used to combine both the Adalines function and is presented [40]. The control mechanism of the Adaline-based synchronisation approach is depicted in Figure 5. Initially, the measured source voltage $v_S(k)$ iscompared with the estimated fundamental voltage in the comparator to generate the error signal $e(k)$. The weight updating algorithm is applied to theresultant error $e(k)$ and is given as in (6).

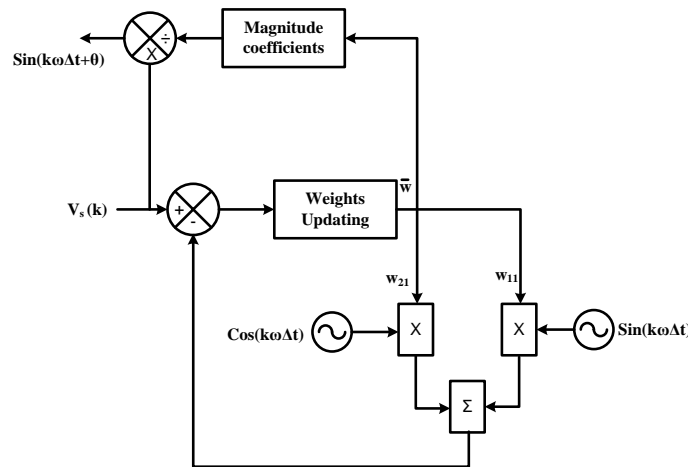$$W(k+1) = W(k) + \frac{\alpha e(k)y(k)}{y(k)^T y(k)}$$

(6)

Figure 5. Block diagram of adaline synchronization technique

The weights W_{11} and W_{21} are used to evaluate the instantaneous fundamental magnitude is given as in (7).

$$V_{Fund_{mag}}(k) = \sqrt{W_{11}^2 + W_{21}^2}$$

(7)

The iteration is repeated continuously until the fundamental magnitude $V_{Fund_{mag}}(k)$ reaches $v_S(k)$. Therefore, the magnitude $v_S(k)$ is generating the desired synchronization signal $\sin(k\omega\Delta t + \theta)$.

Thus, the Adaline synchronization technique is effectively works for balanced source voltage [41]. The Adaline approach can provide the synchronising signal with a single working phase in a single phase system, but it requires three comparable devices in a three phase system. One of the method's main

weaknesses is that it simply doesn't work if the supply voltage is imbalanced or subjected to harmonic disturbances.

2.4. Fundamental component extraction approach

The fundamental component extraction (FCE) approach, which extracts the fundamental component of the source voltage with unity magnitude [42], [43], is another modern SAPF synchronisation technique. This technique's SAPF synchronisation mechanism is identical to that of Adaline. However, even when the supply voltage is uneven or distorted, the FCE technique outperforms the Adaline-based technique [44]. This FCE approach, uses the self-tuning filter (STF) [45], [46], which can efficiently filter out the distortions in the unbalanced signal. The control structure of the basic component extraction approach is shown in Figure 6.
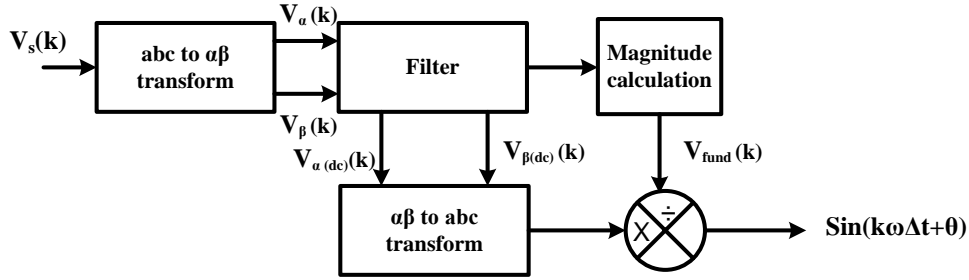

Figure 6. FCE technique

Initially, the source voltage $V_s(k)$ is applied to the Clarke-transformation to extract the process from abc-αβ transformation and is given as in (8).

$$\begin{bmatrix} V_\alpha(k) \\ V_\beta(k) \end{bmatrix} = \begin{bmatrix} V_{\alpha(dc)}(k) + V_{\alpha(ac)}(k) \\ V_{\beta(dc)}(k) + V_{\beta(ac)}(k) \end{bmatrix} \tag{8}$$

Where $V_{\alpha(dc)}(k)$, and $V_{\alpha(ac)}(k)$ are the fundamental and distorted component of V_s in α domain. Similarly, $V_{\beta(dc)}(k)$, and $V_{\beta(ac)}(k)$ are the fundamental and distorted component of V_s in β domain. Then, the αβ domain signal is processed through the filter and converted back to the fundamental sinusoidal signal $V_{sfund}(k)$ using αβ-abc transformation can be given as (9).

$$\begin{bmatrix} V_{sfund,a}(k) \\ V_{sfund,b}(k) \\ V_{sfund,c}(k) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{\alpha(dc)}(k) \\ V_{\beta(dc)}(k) \end{bmatrix} \tag{9}$$

The magnitude of fundamental component of sinusoidal signal $V_{sfund}(k)$ is computed as in (10).

$$V_{sfund_{mag}}(k) = \sqrt{V_{\alpha(dc)}(k)^2 + V_{\beta(dc)}(k)^2} \tag{10}$$

Finally, the desired synchronization signal is obtained by the division of $V_{sfund}(k)$ and $V_{sfund_{mag}}(k)$ to get unity magnitude is given as (11).

$$\sin(k\omega\Delta t + \theta) = \frac{V_{sfund}(k)}{V_{sfund_{mag}}(k)} \tag{11}$$

The FCE technique is most suitable for three phase systems. However, the research to implement this technique to single phase systems can be interesting. Among all these points, it has major drawback of selection of gain parameters of filter.

2.5. Unit vector generation technique

The unit vector generation technique [47] is the most effective technique for the synchronization of SAPF. In this, the unit vectors are generated from the V_s. The control scheme [48] of unit vector generation is shown in Figure 7. The unit vector generation technique has the working principle same as FCE technique, obtained abc-αβ domain using Clarke transformation [49].
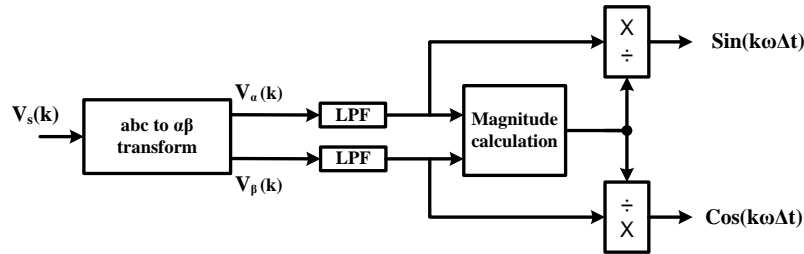

Figure 7. Control scheme of unit vector generation technique

From abc-αβ transformation, the signals $V_\alpha(k)$, and $V_\beta(k)$ represents the sine and cosine signal respectively. These $V_\alpha(k)$, and $V_\beta(k)$ signals are passed through the loop filter (LPF) with the cut-in frequency of 50 Hz, to filter out the higher harmonics present in the voltage source. Then the desired synchronization signals are expressed as:

$$\sin(k\omega\Delta t) = \frac{V_\alpha(k)}{\sqrt{V_\alpha(k)^2 + V_\beta(k)^2}} \tag{12}$$

$$\cos(k\omega\Delta t) = \frac{V_\beta(k)}{\sqrt{V_\alpha(k)^2 + V_\beta(k)^2}} \tag{13}$$

The unit vector generation technique is most suitable for balanced three phase system. The main advantage of this control technique is simple and straightforward without having complex process.

3. CONCLUSION

The phase synchronisation approaches for synchronising SAPF with the power grid have been fully studied and explained in this article. The principle of SAPF is illustrated and the control approach for synchronization of SAPF is presented. The ZCD technique is generating the switching pulses by detecting the zero-crossing point of AC voltage signal. Nonetheless, due to its shortcomings, this approach is still the least recommended for SAPF application. The PLL technique is the most well-known and widely used in SAPF applications. In PLL, the phase detector detects the phase error signal and is passed through the loop filter to supress the high frequency noise signals. The SRF-PLL structure is most preferred synchronisation technique for the applications of three phase SAPF. As a result, more improvements have been made to SRF-PLL allowing it to cope with unbalanced and distorted grid circumstances. Finally, the future research should pay greater attention to hybrid, intelligent, and optimal strategies for effective and reliable synchronisation, particularly under unfavourable and dynamic grid settings.

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