Bulletin of Electrical Engineering and Informatics
Vol. 11, No. 2, April 2022, pp. 901~908
ISSN: 2302-9285, DOI: 10.11591/eei.v11i2.3196

Optimizing frequency synthesizer performance based on passive adder entrenched technique for 4G communication systems

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Article Info

Article history:

Received Sep 6, 2021
Revised Jan 6, 2022
Accepted Feb 21, 2022

Keywords:

2nd order ΔΣ
Frequency synthesizer
Noise shaping
WCDMA

ABSTRACT

Noise in 4G communication systems is a pressing current problem. There are various ways to reduce phase noise. The sigma-delta passive adder entrenched (PAE) approach was chosen for the WCDMA system because it provides a spurious level, phase noise, and low stabilization time. Therefore, for WCDMA applications, this study proposes a frequency synthesizer. It is then suggested that the addition of a passive adder before the modulator's quantizer to eradicate any distortions created as a result of the quantization stage. The design factors for the suggested second order synthesizer for 4G are chosen based on the analytical results for all unit of the suggested system and in accordance with WCDMA specifications. The suggested PAE frequency synthesizer for the application of WCDMA reduces noise exact effectively, according to simulation findings. With this synthesizer, the in-band phase noise is -75 dBc/Hz. For frequency synthesizer simulation, MATLAB (R2020) is utilized.

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1. INTRODUCTION

The most essential network technologies of a mobile communication system's wear fourth generation (4G). All global designs for integrated mobile services are based on GSM and offer data rates of up to 4 Gbps. Wideband coding division multiplexer access (W-CDMA) is a cellular radio access technology on behalf of mobile communication systems (MCS). For MCS, a new frequency band in the 100 GHz region has been set aside. Each channel has a bandwidth of 4 GHz and is used by calls [1], [2]. The data to be transferred is modulated onto a radio frequency (RF) carrier, which is subsequently broadcast over the air, which is common to practically all of these standards [3]. In the receiving end, the received signal is demodulated, and a perfect RF carrier signal must be created. As a result, all wireless communication systems require a frequency synthesizer in the transmitter and receiver. The frequency synthesizer is the most crucial component of any wireless system [4]. A frequency generator is a device that uses a single or several frequency sources to generate one or more frequencies. Voltage-controlled oscillator (VCO) based frequency synthesizes is used in almost all communication systems. The FS is used in the receiver or transmitter of a major radio communication system [5].

A sensitive receiver is required, discriminating and capable of detecting even a small signal among a large number of other, potentially stronger signals. As a result, a good receiver requires a precise local oscillator frequency as well as low noise components. Though, a transmitter must provide a signal with sufficient strength, precise frequency, and clean spectrums [6]. The phase locked loop (PLL) mechanism is used in the majority of RF synthesizes. Three building blocks make up the basic PLL [7].

Charge pump with phase frequency detector (PFD), low pass filter, VOC, and division. On the other side, it raises further concerns. The challenges relating to the segmentation of the digital expression in the feedback channel of the Δ-Σ-DAC will be mathematically analyzed, as well as a proposed solution that uses frequency-shapes to correct this mismatch error [8], [9]. Proposed circuit architecture for the frequency shaping approach will be given in detail. The mathematical analysis and behavioral simulation findings will also be presented [10]. For consecutive approximation register type ADCs, a new noise shaping methodology and a mechanism for dual polarity standardization are suitable. The noise shaping, which includes the inclusion of a switching capacitor, pushes noise to higher frequencies. By using the noise coupling method, the noise shaping quantizer can provide feedback and do extra 1st-order noise shaping on quantization noise. Thus, a noise coupling quantizer shapes the MDC, and two integrators with ring amplifiers 2nd-order noise connected to a DAC modulator [11] is something to be aware of. The inputs are summed and then filtered using a low pass filter at a summing point. In the noise shaping replies, a data weighted averaging approach is employed to generate a cyclic second order response in which the DAC outputs are restricted to one of two states [12]. Abdalsatar [13] presented a 2nd-order noise coupling technique are used an integrated passive adder quantization noise shaping multiple description coding (MDC) of Δ-Σ modulator with two component-based dynamic analog integrators and an embedded Δ-Σ-MDC quantizer with passive adder Two integrators made consisting of ring amplifiers are utilized for 2nd-order noise shaping [14]. The frequency synthesizer's PLL makes the frequency conversion more flexible and the output frequency more steady [15]; the module's thermal problem was also fixed by utilizing a thermistor and changing the operation mode [16]. In this study, we review a new method based on passive adder entrenched (PAE). Simulating the well-known second-order delta- sigma and we find good progress in wave width and the desired results from the experiment and the new method.

2. ANALYSIS DELTA-SIGMA FREQUENCY SYNTHESIZER MODULATOR ARCHITECTURE

The PAE is an independent frequency synthesizer, often known as a digital-to-frequency converter or a direct digital period synthesizer. Circuits that use digital phase accumulators and phase-switching prescalers [9] have some functionality with the PAE. Such as, 8-bit passive adder circuit as summary show in Figure 1. The frequency of the output signal (f_{out}) is generated. The divider's output is a low-frequency signal that is forwarded to PDF. The phase and frequency of the signal are compared at the PFD with an external frequency signal (f_{ref}) generated by a crystal oscillator [17], [18]. The PFD and CP output signals are then low pass filtered, and the filtered signal is delivered to the VOC input to adjust the output signal's frequency. The minimum resolution of an integer synthesizer for a mobile communication system is equal to the reference frequency [19]. Figure 2 illustrations a block diagram of the Phase synthesize interpolation Technique. The output frequency can be varied in frequency increments of reference frequency [20]. A PAE approach is used to produce frequency resolution finer than the reference frequency in order to get finer resolution. Phase interpolation is used in the traditional method to PAE technique synthesizer construction. The PAE frequency synthesizer is well suited for many systemon-chip applications due to its large tuning range and quick response time. When high frequency resolution is desired, the frequency control word could be a fractional or integer value. The PAE synthesizer can be considered as a phase divider when FW is an integer that is complete finer precision than a frequency divider. The PAE modifies the output frequency to achieve improved resolution when FW is a fractional word as refrence N equal 8. The frequency f_{PA} of the output clock F_{out} is provided by the expression as [21]:

$$f_{PA} = \frac{1}{FW.\Delta} = \frac{1}{FW\frac{1}{F_{out}.N}} = F_{out}\frac{N}{FW} \quad (1)$$

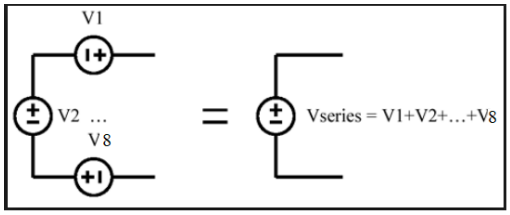

Figure 1. Summary 8-bit passive adder circuit

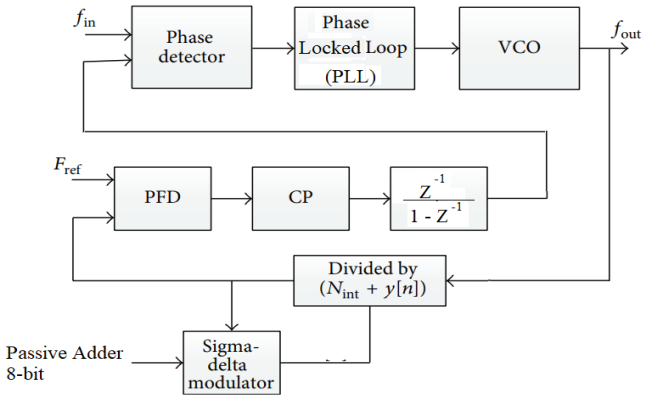

Figure 2. The block diagram of phase synthesizes interpolation technique

The control input to a multi modulus divider is passively added using an accumulator carry-out signal. The DAC is utilized to recompense for the phase error by converting the instantaneous phase error, which is comparative to the accumulator residue, into an equivalent amount of trust-push current [22]. The fundamental drawback of this architecture is the inability to obtain good phase error signal matching between the DAC output and the phase error signal. Because the two signals are handled by distinct circuits whose outputs are summed, this matching is difficult to achieve. Any gain mismatch between the PFD error and the DAC output will result in phantom tones at the PLL output [23]. A delta-sigma modulator is used in the second procedure with PFD.

Figure 3 shows the block diagram of the suggested fractional frequency synthesizer based on the passive adder standard and PLL. The following components make up the synthesizer: A chargepump phase detector, a reference clock, and an N-phase voltage regulated by voltage controlled oscillator (VCO), a Quantizer, a frequency divider, a digital adder with a control frequency word FW, and a register and truncation that convert an 8-bit word to an r-bit word. The frequency of PAE output is f_{PA}. The proposed Δ-Σ is derived from the different and summing nodes in a loop arrangement, where delta (Δ) signifies the difference operation in the input bits and sigma (Σ) denotes the summation or accumulation, as seen in Figure 3. The output of the Δ-Σ modulator in liner models can be stated as [24]:

$$V(z) = \frac{H(z)}{1+H(z)}\ U(z) + \frac{1}{1+H(z)}\ Q(z) \tag{2}$$

Where $H(z) = (z)^{-1})/(1-(z)^{-1})$

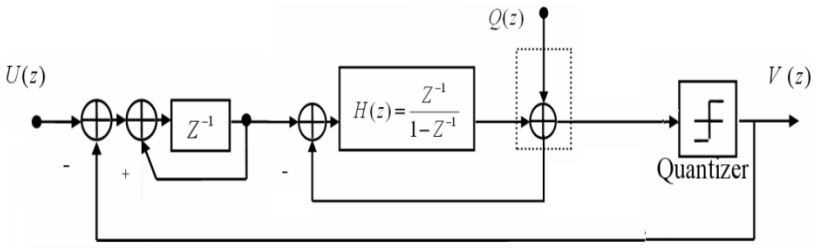

Figure 3. The first order sigma-delta modulator

To determine modulator performance, two transfer functions are used: the system's signal transfer function (STF) besides the noise transfer function (NTF) [25]. The following are the transfer functions:

$$STF(z) = \frac{V(z)}{U(z)}\Big|_{Q(z)=0} = \frac{H(z)}{1+H(z)} = Z^{-1} \tag{3}$$

$$NTF(z) = \frac{V(z)}{Q(z)}\Big|_{U(z)=0} = \frac{1}{1+H(z)} = (1-Z^{-1}) \tag{4}$$

We are substituting in (3) and (4) by (2), the loop output is finded as:

$$V(z) = U(z)\, Z^{-1} + Q(z)(1 - Z^{-1}) \quad (5)$$

The SFT and NFT for high order Δ-Σ modulator as:

$$V(z) = U(z)\, Z^{-1} + Q(z)(1 - Z^{-1})^{N} \quad (6)$$

Where, N denotes the Δ-Σ modulator's order.

3. PROPOSED ΔΣ- PASSIVE ADDER ENTRENCHED QUANTIZER METHOD

As a result, passive adder the operation of adding a random signal to the quantizer's input is enshrined in the Δ-Σ modulator, as seen in Figure 3. The additional random signal is white, and it also becomes noise-shaped like the quantization mistake, reducing the baseband addition noise power. Passive adder's goal is to successfully whiten and decorrlate the quantization error. The output of the firset modulator, as shown in Figure 5 and applied to (3) and (4), is:

$$V_1(z) = U(z) * Z^{-1} + N_{int} * Q_1(z) * Z^{-2} \quad (7)$$

When the first modulotor's *Q1(z)* is connected to the second stage's input, the output is as:

$$V_2(z) = Q_1(z)\, Z^{-1} + N_{int} * Q_2(z)\, (1 - Z^{-1}) \quad (8)$$

Where *Q2(z)* is the second modulator's quantization noise. As a result, the output of the second order modulators of the passive adder can be combined as:

$$V(z) = V_1(z)\, Z^{-2} + V_2(z)\, Z^{-1}(1 - Z^{-1})^2 + Q_L(z)Z^{-1} + Q_2(Z) * (1 - Z^{-1})^2 \quad (9)$$

Where, $Q_L(z)$ is the quantization second level. The quantization noise of the first modulator cancels out, as seen in (9). This greatly enhances the over all modulator's quantization noise reduction. Step response similar to PLLcontaining the 2-nd order low-pass filter with the equivalent parameters, are shown in Figure 4.

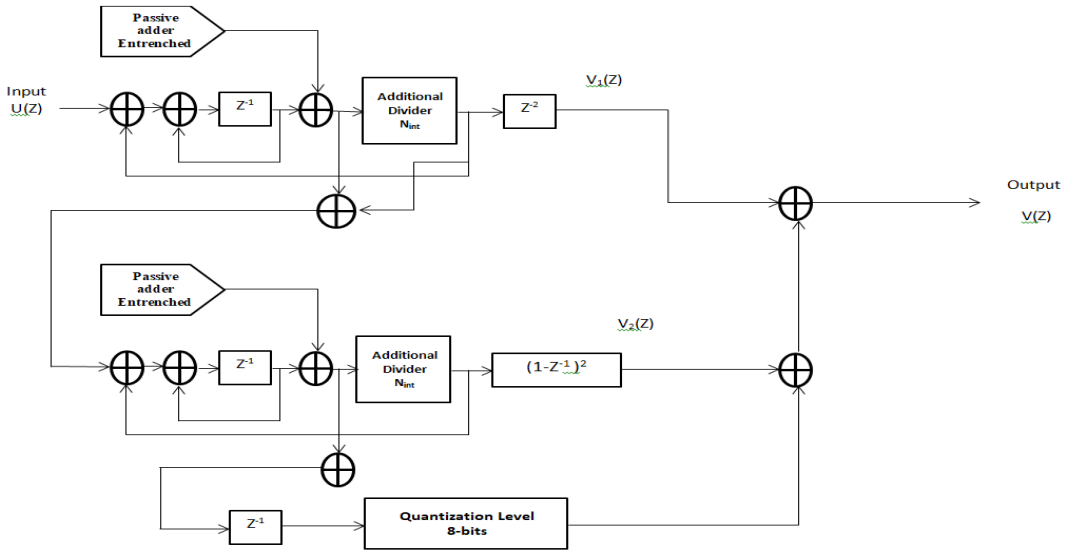

Figure 4. The proposed second-order delta-sigma frequency synthesizer for 4G using a PAE technique

Switching between V1 and V2 in the diagram of such a synthesizer can be used to fine-tune the output frequency. The reference spur problem is an inherent and basic difficulty with PLL frequency synthesizers. As previously mentioned non-idealities of a PFD and up/down current mismatch of a charge

pump provoke periodic charging or discharging processes in the locked state, similar to the loop filter. Periodically disrupts the VCO's control voltage, resulting in the presence of a spurious tone at a reference clock frequency that differs from the VCO output frequency.

4. RESULTS AND DISCUSSION

This section explains the research findings while also providing an in-depth analysis. Table 1 lists the design parameters for PLL synthesis for WCDMA applications, which are either chosen from WCDMA standards or based on the result analysis of each component of the proposed passive adder quantizer system. Figure 5 also depicts the simulation result of the suggested frequency synthesizer using a second-order delta-sigma PAE technique. Using a PAE technique, the quantization noise 2nd order modulator is perfectly negated. The delta-sigma frequency synthesizer, on the other hand, is recommended for removing quantization noise and spurs. However, The delta-sigma frequency synthesizer, on the other hand, is recommended for removing quantization noise and spurs. When compared to the signal-loop 2nd order arrangement shown in Figure 6, the net improvement in quantization noise reduction is 7 dB. At 1 MHz and 2 MHz offset frequencies, phase noise performance is -98.7 dBc/Hz and -136 dBc/Hz, respectively, translating to a 54m Vrms. For multiplication factors of 57 MHz input reference clock, the waveforms of the multiplied output clocks were PAE. With a reference frequency as low as 50 MHz, the suggested frequency multiplier can provide doubled clock signals from the input clock. A 60 MHz input reference clock is multiplied three times at the output, as shown in Figure 5 and Figure 6.

Table 1. Parameters of the proposed passive adder quantizer based on ΔΣ-2nd modulators

Parameter/factor	Description/value
Type filter	Butterworth passive
Accumulator bit	8 bit
Switch noise (KT/C)	54 *rms*m*V*
Noise figure	14 *rms* m*V*
Finite Dc gain	(60) dB
VOC sensitivity	0.45 GHz/V
VOC Frequency	2 MHz
RF channel bandwidth	12.5 MHz

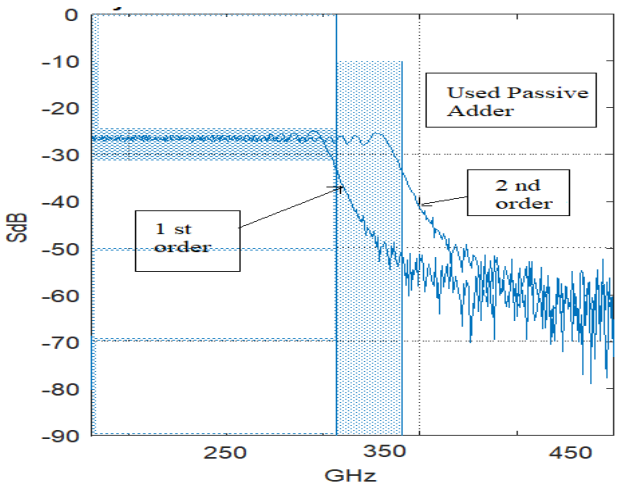

Figure 5. The noise spectrum quantization second-order delta-sigma by a PAE method

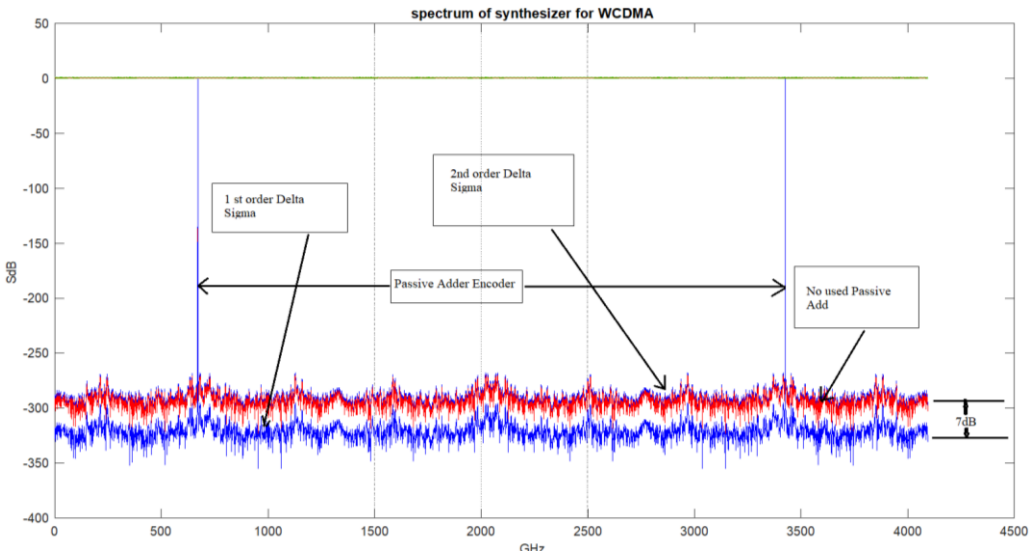

Figure 6. The different 7 dB between 1st and 2nd noise spectrum quantization

Figure 7 depicts the final 2nd order simulation result for a PAE synthesizer for WCDMA. Broadband noise is considerably minimized, resulting in high percentage spur rejection at the PLL output spectrum. As demonstrated in Figure 7 synthesizes overall phase noise performance is good, meeting the equivalent of WCDMA requirements at 2.46 GHz while also meeting the decreased spurious aim. Furthermore, the results reveal that the proposed technology is successful in reducing phase noise and spurs. The net improvement in phase noise is up (6 dB/Hz) in band as compression with frequency references that have attained similar specifications to our research, so that, it is easier to compare with frequency and latest references have been taken into account. The final phase noise findings of the suggested ΔΣ-2nd modulators based passive adder are summarized in Table 2 and compared to different reference. The performance of PAE frequency synthesizers is compared in Table 2. In comparison to [10], [17] the suggested frequency synthesizer obtained the smallest area, power, and output frequency range in 0.23 mw and 57MHz process technology. We increase noise figure (14 rms mV) performance compared to [14]'s flying-adder structure by setting the worst case in the fractional section of the frequency control word. This technique also outperforms [26], [27]'s two-path PLL in 12.5 MHz bandwidth. A tone is created at a specific frequency to measure the spurious-free dynamic range (SFDR) of a signal generator. The amplitude of the basic tone and the amplitude of the next highest tone are then measured using a spectrum analyzer [28]. This is usually one of the harmonics. It is simple to calculate SFDR using decibels:

$$SFDR = Ampltiude\ of\ Fundmental\ (dB) - Ampltiude\ of\ larcgest\ spur\ (dB) \quad (10)$$

This works also has SFDR in dB based on (10) performance better than the rest of the techniques explained in the references referred to in Table 2.

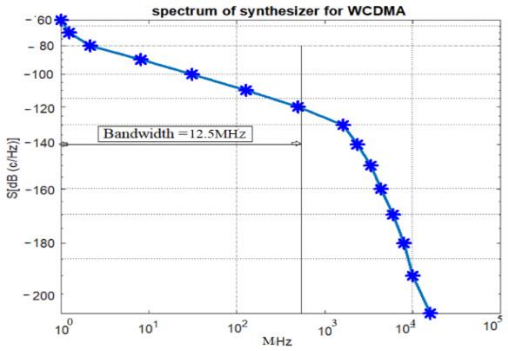

Figure 7. Output spectrum of synthesizer of PAE technique for WCDMA

Table 2. Summary of simulation result compared with of previous works

Factors	Raheema and et. [17]	Yu and et. [10]	Khleaf and et. [14]	Nahar and et. [This work]
Output frequency (GHz)	1.965	1.97	2.1	2.46
In band phase noise (dB/Hz)	-96	-92	-102	-136
Reference frequency (MHz)	85	26	39	57
Sampling rate (MS/s)	25	100	100	100
Loop bandwidth (MHz)	8.9	10.9	11.125	12.5
Quantizer	1 bit	4 bit	8 bit	8 bit
Power (mW)	-	0.52	0. 34	0.23
SFDR (dB)	172.5	169.2	179.9	190

5. CONCLUSION

The second-order PAE technique frequency synthesizer is designed to generate 2.46 GHz with phase noise -136 dB/Hz phase noise -145 dB/Hz in and out of band accordingly. In addition, PAE technique frequency synthesizer is selected to WCDMA system to obtained bandwidth roughly 12.5 MHz. Then it has the advantage of a faster setup time and a smaller step size than an integral PLL. Using a 2nd order delta-sigma passive adder, the modulator's quantization noise is perfectly neutralized. Because it uses just one reference source and generates offset-frequency signals from a PLL-based frequency Synthesizer, the proposed design has significant cost, low complex chip area, and power consumption advantages over current offset-frequency PLL systems.

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